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EXAMINER	
TRAN, TRANG U	

ART UNIT	PAPER NUMBER
2622	

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,271	GREENBERG, ROBERT Y.	
	Examiner	Art Unit	
	Trang U. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed Aug. 25, 2006 have been fully considered but they are not persuasive.

In re pages 5-7, applicant argues, with respect to claim 1, that the ADC 130 of the prior art is not the claimed edge detector circuit, the digital data analysis circuit 140 is not the claimed phase detector circuit, the phase adjuster 50 of Cappels is not the claimed phase adjust circuit because the phase adjuster 50 generates a single adjusted pixel sampling clock 64 which is in contrast with the recited plurality of delayed clock signal generated by the phase adjust circuit, that the motivation to combine is not present in either Cappels or the APA, and, even if motivation to combine was present (it is not), the combination of Cappels' phase adjuster 50 with the APA would not produce an operable system because the APA circuit does not use any delayed clock signals obtained by delaying the phase locked loop clock.

In response, the examiner respectfully disagrees. First at all, claim 1 recites "**an edge detector circuit to generate an edge pulse signal corresponding to a transition of an analog data signal above a predetermined threshold responsive to a pixel clock**". It is noted that the ADC 130 of the prior art **also generates an edge pulse signal corresponding to a transition of an analog data signal above a predetermined threshold responsive to a pixel clock.** Thus, the claimed "an edge detector" is anticipated by the "ADC 130" of the admitted prior art.

Claim 1 also recites "**a phase detector circuit to generate a phase adjust signal responsive to a phase of the phase locked loop clock and the edge pulse signal**". As discussed above the output of the ADC 130 is the claimed edge pulse signal and the circuit 100 of the admitted prior art is **an feedback circuit** with a PLL circuit 112. The digital data analysis circuit 140 generates a phase adjust signal (138) responsive to a phase of the phase locked loop clock (PLLCLK 122 and the circuit 100 is the feedback circuit) and the edge pulse signal (134). Thus, the claimed "a phase detector circuit" is anticipated by the digital data analysis circuit 140 of the admitted prior art.

Claim 1 recites "the phase adjust circuit generates a plurality of delayed clock signals by delaying the phase locked loop clock". It is noted that claim 1 does not specifically recite that the phase adjust circuit **simultaneously** generates a plurality of delayed clock signal by delaying the phase locked loop clock but it could **sequentially** generates a plurality of delayed clock signal by delaying the phase locked loop clock. Cappels phase adjuster 50 **sequentially generates a plurality delayed pixel sampling clock 64 that matches the phase of the video signal 52.**

Cappels is cited only to suggest the phase adjuster 50 which produces an adjusted pixel sampling clock 64 that matches the phase of the video signal 52. The adjusting pixel sampling clock 64 as taught by Cappels has similar application whether the signal is the pixel sampling clock 64 or the phase locked loop clock. A reference must be considered not only for what it expressly teaches, but also for what it expressly teaches, but also for what it fairly suggests. In re Burckel, 592 F.2d 1175, 201 USPQ 67

(CCPA 1979). The artisan is presumed to know something about the art apart from what references literally disclose. In re Jacoby, 309 F.2d 513, 135 USPQ 317 (CCPA 1962). The examiner believes the artisan would have recognized the obviousness of adjusting the clock signal.

As discussed above, there is motivation to combined the references as proposed and the Cappels' phase adjuster 50 has similar application whether the signal is the pixel sampling clock 64 as taught by Cappels or the phase locked loop clock. The proposed combination of the references would produce an operable system.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 5-6 and 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cappels, Sr. (US Patent No. 5,731,843) in view of Levantovsky et al. (US Patent No. 6,522,365 B1).

In considering claim 1, Cappels, Sr. discloses all the claimed subject matter, note 1) the claimed a phase locked loop circuit to generate a phase locked loop clock responsive to a reference signal is met by the pixel sampling clock 55 which is a conventional phase-locked loop using a programmable divider and coupled to the horizontal sync pulse (Fig. 3, col. 4, lines 35-42), 2) the claimed an edge detector circuit to generate an edge pulse signal corresponding to a transition of an analog data signal

is met by the differentiator 52 and the threshold detector 44 which is function together to detect voltage transitions between pixel instructions, also called pixels edges (Fig. 3, col. 4, lines 42-59), 3) the claimed a phase detector circuit to generate a phase adjust signal responsive to a phase of the phase locked loop clock and the edge pulse signal is met by the phase comparator 46 and the microprocessor 48 (Fig. 3, col. 4, line 60 to col. 5, line 27), and 4) the claimed a phase adjust circuit to generate a pixel clock responsive to the phase adjust signal and the phase locked loop clock, wherein the phase adjust circuit generates a plurality of delayed clock signals by delaying the phase locked loop clock is met by the phase adjuster (phase shift of Fig. 4) 50 which produces an adjusted pixel sampling clock 64 that matches the phase of the video signal 52 (Figs. 3 and 4, col. 5, line 15 to col. 6, line 31).

However, Cappels, Sr. explicitly does not disclose the claimed an edge detector circuit to generate an edge pulse signal responsive to a pixel clock.

Levantovsky et al teach that referring to FIG. 2, a pixel clock 50 used in sampling the active video portion 36 of an analog signal 10 and converting to a digital signal (not shown) for display on a digital display (e.g., a flat panel display (FPD)) is shown in various phase relationships with the active video signal 10 (Fig. 2, col. 4, line 48 to col. 5, line 51) and the edge detection module 64 has an input 76 couple to the output 74 of the ADC 62 and an output 78 to provide the pixel coordinates of the earliest on-transition and latest off-transition times for each video frame (Fig. 7, col. 6, line 55 to col. 7, line 19).

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the pixel clock used in sampling the active video portion of an analog signal and the edge detection module as taught by Levantovsky et al into Cappels, Sr.'s system in order to accurately adjusting the frequency and phase of the pixel clock.

In considering claim 3, the claimed wherein the reference signal is a horizontal synchronization signal is met by the pixel sampling clock 55 which is a conventional phase-locked loop using a programmable divider and coupled to the horizontal sync pulse (Fig. 3, col. 4, lines 35-42 of Cappels, Sr.).

In considering claim 5, the combination of Cappels, Sr. and Levantovsky et al discloses all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the threshold is programmable. The capability of using the threshold is programmable is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the old and well known of using the threshold is programmable into the combination of Cappels, Sr. and Levantovsky et al's system in order to accurately detect the edge pulse signal because programmable device can easily adjust the threshold level to appropriate level.

In considering claim 6, the claimed wherein the edge detector generates an edge pulse corresponding to a rising, falling, or both rising and falling edges of the analog data signal is met by the voltage transition location 20 which occurs between a change

in voltage levels and between discrete pixel intensities 19 on video signal 12 (Fig. 1, col. 3, lines 6-43 of Cappels, Sr.).

In considering claim 11, Cappels, Sr. discloses all the claimed subject matter, note, 1) the claimed wherein the phase detector comprises: a phase hit detector to generate a plurality of phase hit enable signals corresponding to the plurality of delayed clock signals and assert one of the phase hit enable signals responsive to the edge pulse signal is met by the hit detection process (Fig. 5, col. 4, line 60 to col. 5, line 27 and col. 6, line 58 to col. 7, line 37), and 2) the claimed a phase hit counter to count asserted phase hit enable signals for each of the delayed clock signals over a predetermined time is met the microprocessor 48 stores in memory 49 a number representing the total hits for that specific phase (col. 5, lines 3-27).

In considering claim 12, the combination of Cappels, Sr. and Levantovsky et al discloses all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the predetermined time is a number of image scan lines. The capability of using the predetermined time is a number of image scan lines is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the old and well known of using the predetermined time is a number of image scan lines into the combination of Cappels, Sr. and Levantovsky et al's system since it merely amounts to selecting an alternative equivalent edge detector.

In considering claim 13, the claimed wherein the phase hit detector comprises: a plurality of flip-flop circuits corresponding to the plurality of delayed clock signals

adapted to generate a corresponding plurality of phase out signals, and a comparison circuit to comparing the plurality of phase out signals is met by the comparator 99 which includes a one-shot pulse generator 81 and latches (flip-flops) 82 and 84 (Fig. 5, col. 6, line 58 to col. 7, line 37 of Cappels, Sr.).

In considering claim 14, the claimed wherein the comparison circuit compares adjacent phase out signals is met by the comparator 99 which includes a one-shot pulse generator 81 and latches (flip-flops) 82 and 84 (Fig. 5, col. 6, line 58 to col. 7, line 37 of Cappels, Sr.).

In considering claim 15, Cappels, Sr. discloses all the claimed subject matter, note 1) the claimed wherein the phase hit counter comprises: an enable signal to enable counting of asserted phase hit enable signals is met by the Q-output pulse 108 from the one-shot pulse generator 81 is true, data line 112 is set high, indicating that a "hit", a sampling edge in close temporal proximity to a video transition, has taken place (Fig. 5, col. 6, line 58 to col. 7, line 37), and 2) the claimed a clear signal to clear the phase hit counter is met by the NOT-Q output 118 of one-shot pulse generator 81, the latch 82 is reset to await for the next edge detection (Fig. 5, col. 6, line 58 to col. 7, line 37) .

In considering claim 16, the claimed comprising: a phase count analysis circuit to generate phase and frequency adjust signals by analyzing the count of asserted phase hit enable signals is met by the microprocessor 48 which calculates a hit percentage for each varies phase and the hit percentage is the number of hits for a given number of video edges at a given phase to obtain which phase is the maximum number of hits, then the microprocessor 48 can determine the phase of the sampling clock with respect

to the horizontal synchronization pulse that will provide the optimum sampling of the incoming video signal 52 (Fig. 4, col. 5, line 15 to col. 6, line 31 of Cappels, Sr.).

In considering claim 17, the claimed comprising an auto calibration circuit to align the analog data signal with the pixel clock is met by the automatically adjusting the pixel sampling clock frequency and phase to match the frequency and phase of the pixel clock used to generate an incoming video signal (col. 1, lines 60-64 of Cappels, Sr.).

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cappels, Sr. (US Patent No. 5,731,843) in view of Levantovsky et al. (US Patent No. 6,522,365 B1), and further in view of Koike et al (US Patent No. 6,538,648 B1).

In considering claim 2, the combination of Cappels, Sr. and Levantovsky et al discloses all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the phase locked loop circuit comprises: a phase detector adapted to receive the reference signal; a loop filter coupled to the phase detector; a voltage controlled oscillator coupled to the loop filter; a feedback loop adapted to receive the phase locked loop clock and provide a feedback signal responsive to a frequency adjust signal. Koike et al teach that the PLL circuit 40 comprises a phase detection unit 41, an LPF (Low pass Filter) 42, a VCO (Voltage Control Oscillator) 43, and a frequency divider 44, as is well known (Fig. 2, col. 6, lines 46-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the old and well known PLL as taught by Koike et al into the combination of Cappels, Sr. and Levantovsky et al's system in order to generate the clock signal that is synchronized with the local frequency oscillator.

5. Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cappels, Sr. (US Patent No. 5,731,843) in view of Levantovsky et al. (US Patent No. 6,522,365 B1), and further in view of Ichiraku (US Patent No. 6,097,379).

In considering claim 7, the combination of Cappels, Sr. and Levantovsky et al discloses all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the phase adjust circuit adjusts the phase of the pixel clock by delaying the reference signal. Ichiraku teaches that as is shown in Fig. 3, the phase adjusting circuit 2 of the present invention is provided with: a sampling clock generating circuit for detection 21, into which a standard clock (PCLK) which is synchronized with a horizontal synchronizing signal is inputted, and which divides this standard clock (PCLK) into a number m (a positive integer) of standard clocks, and which applies, with respect to these standard clocks, a delay amount proportional to the amount of the cycle thereof divided by m, and which generates and outputs, in stages, a number m of sampling clocks for detection (DPCLK [0,1,2,...,m]) having different phases (Fig. 3, col. 8, line 43 to col. 9, line 40). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the delay clocks (DPCLK [0,1,2,...,m]) having different phases as taught by Ichiraku into the combination of Cappels, Sr. and Levantovsky et al's system in order to accurately produce the sampling clock signal having an appropriate phase for sampling pixel data of the video signal.

In considering claim 8, the combination of Cappels, Sr. and Levantovsky et al discloses all the limitations of the instant invention as discussed in claim 1 above,

except for providing the claimed wherein the phase adjust circuit adjusts the phase of the pixel clock by delaying the phase locked loop clock. Ichiraku teaches that as is shown in Fig. 3, the phase adjusting circuit 2 of the present invention is provided with: a sampling clock generating circuit for detection 21, into which a standard clock (PCLK) which is synchronized with a horizontal synchronizing signal is inputted, and which divides this standard clock (PCLK) into a number m (a positive integer) of standard clocks, and which applies, with respect to these standard clocks, a delay amount proportional to the amount of the cycle thereof divided by m, and which generates and outputs, in stages, a number m of sampling clocks for detection (DPCLK [0,1,2,...,m]) having different phases (Fig. 3, col. 8, line 43 to col. 9, line 40). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the delay clocks (DPCLK[0,1,2,...,m]) having different phases as taught by Ichiraku into the combination of Cappels, Sr. and Levantovsky et al's system in order to accurately produce the sampling clock signal having an appropriate phase for sampling pixel data of the video signal.

In considering claim 9, Ichiraku discloses the claimed wherein the phase adjust circuit comprises: a clock delay circuit to generate a plurality of delayed clock signals by delaying the phase locked loop clock is met by the delay clocks (DPCLK [0,1,2,...,m]) having different phases (Fig. 3, col. 8, line 43 to col. 9, line 40 of Ichiraku), and the claimed a multiplexer to select one of the plurality of delayed clock signals as the pixel clock responsive to a phase adjust signal is met by the selecting circuit 22 which selects the appropriate sampling clock for detection and outputs this as the sampling clock

(SCLK) to the pixel data sampling circuit (Fig. 3, col. 8, line 43 to col. 9, line 40 of Ichiraku).

In considering claim 10, the claimed wherein the clock delay circuit comprises an n-stage delay locked loop, each stage generating a corresponding delayed clock phase, each delayed clock phase being 360/n degrees out of phase is met by the delay clocks (DPCLK [0,1,2,...,m]) having different phases (Fig. 3, col. 8, line 43 to col. 9, line 40 of Ichiraku).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (571) 272-7358. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 12, 2006

Trang U. Tran
Primary Examiner
Art Unit 2622